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THE GROWTH OF EPITAXIAL GaAs AND GaAlAs ON SILICON SUBSTRATES BY OMVPE

9th QUARTERLY REPORT
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CONTENTS

1. INTRODUCTION

This report covers the reporting period September to November 1988, quarter 9 in the program.

1.1 Planned Work

The planned work for quarter 9 was as follows:-

(1) Growth of GaAs on Si FETs and GaAs/GaAs control specimens.
(2) Processing, assessment and testing of discrete devices fabricated from the material grown in (1).
(3) Design and fabrication of low complexity structures containing more than one device function.
(4) Continue experimental growths of GaAs on profiled silicon substrates.
(5) Continue low temperature substrate preparation experiments.
(6) Selective area epitaxy of GaAs on silicon.
(7) Defect reducing experiments using repetitive anneal-grow sequences.
(8) Use of SLS in conjunction with (7).

1.2 Summary of Progress

(1) Growth of GaAs on Silicon FETs and GaAs FET Structures

Further heteroepitaxial and homo-epitaxial FET structures have been grown and assessed. CV profiles and mesa isolation tests have revealed difficulties in obtaining GaAs buffer layers with sufficiently high resistance to provide adequate mesa isolation to enable FETs to be processed to completion.

(2) Growth of GaAs on Profiled Silicon Substrates

A further series of silicon substrates have been submitted for processing to give linear features orientated in the [110], [1$\bar{1}$0], [010] and [100], directions.

(3) Low Temperature Cleaning

Low temperature plasma cleaning experiments have been continued using hydrogen and hydrogen/arsine mixtures. Successful epitaxial growth of GaAs on silicon cleaned at 900^{0}C has been demonstrated, but the technique is not yet optimised to give reproducible results.

(4) Selective Area Epitaxy

Photolithography and wet chemical etching have been used to prepare silicon nitride and silica masks on 3" diameter silicon substrates. The exposed substrate surfaces consist of a range of circular and rectangular features for assessment of growth behaviour on the mask material and in the window areas.

(5) Cyclic Thermal Annealing

Preliminary experiments using repetitive growth-anneal sequences during the deposition of GaAs on silicon have been undertaken. Assessment of this material will be reported in quarter 10.

(6) Cathodoluminescence Studies

Cathodoluminescence studies of GaAs on silicon have been carried out, showing changes in CL peak positions related to tensile strain in the region of thermal mismatch cracks.

(7) Design and Fabrication of Low Complexity Structures containing more than one device function

Preliminary discussions have been undertaken with the silicon processing area regarding compatibility of processed silicon devices with the temperature cycle and exposure to reactants during MOCVD growth. Development of reproducible low temperature silicon substrate cleaning is crucial to any further advancement with these experiments.

2. MATERIALS GROWTH

2.1 Growth of High Resistance Gallium Arsenide on Silicon for FET Buffer Layers

Previously we reported MOVPE growth of undoped GaAs on semi-insulating GaAs substrates with carrier concentrations in the range $8x10^{13}cm^{-3}$ to $2x10^{14}cm^{-3}$, and μ_{77K} mobilities >100,000 $cm^2V^{-1}s^{-1}$, using an adduct purified TMG source.

However when this source was used for the growth of GaAs on silicon FET structures there was a general trend for the GaAs on silicon buffer layer to be more highly doped than the control specimen homostructure buffer, typically $2x10^{15}cm^{-3}$ in comparison with $2x10^{14}cm^{-3}$ in the homostructure, see fig. 2.1.1. We also observed that the background carrier concentration in the homoepitaxial FET buffer varied from $2x10^{14}$ to $8 \times 10^{14}cm^{-3}$.

At this stage in the program a new extraction cabinet incorporating several additional safety features was installed in the MOVPE system. During this modification the high pressure dilute (15%) arsine source was exchanged for a low pressure pure liquid arsine source.

At this time the TMG source also had to be replaced since the original source, which gave high mobility material, had become exhausted.

Using the new arsine and TMG sources a series of thick ~10nm GaAs layers was grown using undoped semi-insulating substrates.

Hall measurements on these specimens showed that the material grown from the new group III and group V sources was unsuitable for FET buffers with donor concentrations in the range $5x10^{14}cm^{-3}$ to $1x10^{15}cm^{-3}$ and corresponding 77K mobilities of 30,000-50,000$cm^2V^{-1}s^{-1}$. It was eventually established that this deterioration in material quality was associated with silicon in the new TMG source. The source was replaced and growth of material with 77K mobilities of 100,000 $cm^2V^{-1}s^{-1}$ re-established.

In the course of these experiments it was observed that the Hall measurements were, in some cases, affected by substrate conversion during the GaAs thermal clean at 850^{0}C. This problem was avoided by carrying out the thermal clean at lower temperatures 720-750^{0}C, by growing the undoped layer at 650^{0}C, and by choosing GaAs substrate material which was known to be more thermally stable.

The variation observed in background doping of the control homo-epitaxial FET buffers may be explained in part by type conversion of the GaAs substrates used as test pieces during the growth of the GaAs on silicon FETs since this material was baked at 850^{0}C prior to growth of the FET buffer layer. This could also be the reason why one of the homoepitaxial FET test pieces failed to pass the Mesa isolation test (see section 3).

2.2 Growth of GaAs on Si FET Structures

FET structures were grown on high resistance silicon substrates using the two step procedure described in quarter 8, i.e. growth of the base layer, followed by growth of the FET structures in a separate growth run on a clean and pre-conditioned susceptor.

Homoepitaxial FET structures were grown simultaneously in the same reactor, as control specimens.

These structures were assessed by mercury probe CV profiling, electrochemical profiling, and by device processing to the mesa isolation test stage.

These assessments also revealed inconsistencies in the quality of the undoped GaAs FET buffer layer.

Device processing and assessment of this material is described in detail in section 3.

2.3 Growth on Profiled Substrates

A further series of silicon substrates have been prepared for growth.

The substrates were cleaned using the RCA technique, and then a ~2000Å layer of Si_3N_4 deposited. Photolithography was then used to define stripes in the nitride, varying in width from 7μm to 100μm with a separation of approximately 300μm. The wafers were etched in 2% HF in HNO_3 to leave the stripe features raised by 2μm above the wafer surface. The stripes were orientated in the two orthogonal [110] directions, i.e. parallel and perpendicular to the major substrate flat, and at 45^0 to the major flat, as shown in Fig. 2.3.1. Fig. 2.3.2 shows a cross-section through this structure. A similar set of substrates has been prepared using reactive ion etching in CF_4.

The intention here is to study the effect of stripe orientation and stripe preparation on the quality of the epitaxial layer growth, and the results will be reported later after growth and assessment of these structures.

2.4 Low Temperature Silicon Surface Cleaning Experiments

Experiments reported previously showed that GaAs which was visually specular with X-ray FWHM of 200 arc secs could be grown on silicon which had been cleaned using a low pressure OMVPE apparatus at 950^0C at 100 torr and an r.f. generated hydrogen plasma. Recent work has been aimed at improving the reproducibility of this and if possible lowering the cleaning temperature further.

Experiments

The r.f. generated plasma obtained by using our R.F. heated susceptor at low pressure, referred to in quarter 8, was found to be unstable and the apparatus was modified to incorporate a microwave generated plasma situated at the inlet tube, and the reactor tube redesigned to incorporate a susceptor which could support two substrates, one horizontally and the other vertically. See Fig. 2.4.1. The vertically supported substrate orientation

was intended to ensure better interaction between the substrate and the microwave generated plasma which travelled down the reactor from the inlet tube. Silicon substrates were cleaned using a plasma generated in hydrogen/arsine mixtures with a reactor pressure of approximately 5 Torr, and substrate temperatures of 900-950^{0}C.

However, these results were not obtained consistently and further investigation of the silicon surface after exposure to the plasma, using Auger electron spectroscopy showed the presence of oxide on the surface, and examination of the quartz inlet to the reactor showed evidence of degradation of the quartz in the vicinity of the microwave cavity, suggesting that the hydrogen plasma was capable of reducing the quartz inlet tube of the reactor and the resulting volatile silicon monoxide was then deposited on the substrate surface thus giving poor nucleation of the GaAs. Experiments are in hand to deploy argon or helium and hydrogen mixtures to eliminate this effect by broadening the discharge and reducing the power density at the inlet tube wall.

Auger analysis of the surface of thermally cleaned silicon substrates also showed that there was some contamination due to leaks upstream relative to the reactor inlet. The apparatus has been modified to eliminate these leaks. Further experiments on thermal cleaning in hydrogen/arsine mixtures are currently under way, and will be reported later.

After cleaning, the initial GaAlAs/GaAs SLS was grown at 400^{0}C, followed by growth of 3-4μm of GaAs, Fig. 2.4.2. This material was assessed by visual inspection, interference contrast optical microscopy, and X-ray diffraction. The best growths were visually specular, with surface morphologies similar to those obtained in the atmospheric pressure MOVPE system, see Fig. 2.4.3, and a minimum double crystal diffraction peak FWHM of 173 arc secs, Fig. 2.4.4.

2.5 Comparison of Growth on (001) and 3° off (001) Substrates

We have usually used silicon substrates which are orientated (001) ± 0.5° for MOVPE of GaAs on silicon. Surface cleaning and surface reconstruction [1] are achieved by heating the substrate in excess of 1100°C for periods of up to 30 minutes. This technique has resulted in the growth of GaAs on silicon which is free from antiphase domains and stacking faults/ microtwins, implying that the appropriate surface reconstruction has taken place and that the substrate surface is clean. It has been reported [2] that substrate surface reconstruction/step doubling will take place at lower temperatures, e.g. ~900°C if (001) silicon substrates misorientated by 3-4° towards the furthest {110} are used.

For each growth experiment two (001) substrates were included. One on orientation and one tilted 3° off towards the furthest {110} were placed in the reactor for simultaneous growth of gallium arsenide. In one experiment case the substrate thermal clean and surface reconditioning were carried out at 900°C and in the other experiment the substrates were subjected to the usual thermal clean and reconstruction at 1100°C. The structure grown was the first step FET structure containing two bands of GaInAs/GaAs SLS [3].

For the 900°C treatment both wafers were grey, the surface morphology was rough, and X-ray diffraction rocking curves showed broad peaks >500 arc seconds indicative of poor crystal quality.

For the 1100°C treatment, the on orientation wafer had a specular surface, the off orientation wafer was slightly hazy. X-ray diffraction rocking curves gave values of 297 arc secs for the on orientation material and 253 arc secs for the off orientation material.

Optical microscopy showed significant differences between the surface morphologies of "as grown" wafers, Fig. 2.5.1. Growth on exact (001) shows isotropic islands with ~10-15μm sizes giving comparatively smooth surfaces. Growth on 3° off orientation substrates shows anisotropic islands 2-4μm along [110] and ~6-8μm along [$\bar{1}$10]. Terracing of these islands results in rougher surface topography.

Defect densities in the GaAs epilayers as measured by etch pit densities were identical within experimental error limits for on-orientation and 3^0 off orientation substrates, Fig. 2.5.2.

CV profiles indicate lower background doping for unintentionally doped GaAs grown on 3^0 off orientation material, Fig. 2.5.3.

These experiments are continuing, in order to determine whether the lower background doping observed for the growth on 3^0 off substrates is a consistent feature of growth on off-orientation substrates.

Further investigation of the substrate thermal clean procedures are being carried out to establish whether low temperature cleaning techniques, compatible with those used in MBE growth of GaAs on silicon, are feasible in an atmospheric pressure MOVPE system. See section 2.4.

2.6 Cathodoluminescence

2.6.1 Introduction

In the 6th Quarterly Report some preliminary examinations of epitaxial layer OA 423 were presented. The structure of OA 423 is given in Fig. 2.6.1. Two features of this specimen were discussed: firstly the configuraton of etched cracks (resulting from the thermal contraction mismatch between GaAs and Si) and secondly the visibility of cross-hatch patterns. In both cases the effects of etching, using the Wright etch, were found to be beneficial for making visible features which are difficult to resolve in as-grown material using an optical microscope, even when employing Nomarski inteference contrast. In particular, the faintly visible cross-hatch pattern on the unetched surface improved in visibility as the etch time was increased (from 10 to 22 seconds, corresponding to etch depths of 1μm and 2.2μm respectively). This suggested that the cross-hatch structure occupied a finite extent of the epilayer, up to and including the outer surface. For this reason it was proposed that further work should be carried out, including the use of low temperature cathodoluminescence (CL) techniques, to examine this possibility. It will be seen that in addition to information regarding the

cross-hatch structure CL was able to demonstrate directly that tensile stress in the epilayer was reduced in the vicinity of the <110> cracks.

2.6.2 Experimental Details

The specimen preparation for optical and CL examinations was straightforward. A rectangular strip ~25mm x 5mm was cleaved out of the wafer and successively masked to give regions which were Wright etched for 10, 22, 32, and 44 secs. Observations were made close to the boundaries between two differently etched areas. After a set of Nomarski interference contrast micrographs had been obtained the strip was cut in half and the two strips mounted with silver dag on a copper block which could be liquid helium cooled in a Cambridge S150 scanning electron microscope (SEM). The scanning CL was carried out in the SEM operating at 20kV with a .5nA probe current. Light was collected with Hexland Instruments high-efficiency optics and detected with an S20ER photomultiplier tube, which responds to band edge emission at 1.51eV to 1.49eV, but not the broad deep-level emission at ~0.68eV to 0.63eV. The SEM was used to record micrograph-like maps of the band edge emission from each etched area at a sample temperature of ~10K. In addition, because biaxial stress will alter the bulk GaAs 1.51eV (8210nm wavelength) emission, spectra from different areas of the unetched region were also determined.

2.6.3 Results

Fig. 2.6.1 shows the etch depths predicted to be reached after the various etch times, assuming that the etch rate is constant at $0.1\mu ms^{-1}$. This value is based on previous step profile measurements for GaAs/Si epilayers subjected to a range of etch times and is probably reproducible to ±10%, although the effects of repeated etch treatments for different times may differ from a single treatment for the equivalent total time. Wright etched surfaces and band edge low temperature (10K) CL emission maps for the various etched regions are shown in Figs. 2.6.2-2.6.4. Detailed descriptions of the information which can be obtained by close scrutiny and measurements are presented in Table 2.6.1. These results will be discussed in the following section.

The CL emission maps clearly demonstrate that here are regions of enhanced emission (lighter contrast) surrounding the thermal mismatched cracks along <110>. A publication by Jacobi et al (1987) [4] had indicated that variations in photoluminescence (PL) and CL peak wavelengths (λ) occurred across 'cells' in MOVPE and MBE GaAs on Si, the cells being defined by orthogonal cracks, and it was proposed that the peak λ shifts resulted from in-plane stress changes in the vicinity of the cracks. We have attempted to reproduce these results for layer OA 423, using a region of the as-grown and unetched layer containing widely spaced cracks. Fig. 2.6.5. shows how the peak CL wavelength alters with position of the exciting beam with reference to one of the thermal mismatch cracks. It should be noted that the peak heights do not represent the peak intensities on this graph. These three peaks are shown to exemplify the peak shift effect: in fact nine positions from 60μm to 0μm from the crack were measured, both for peak position and peak intensity. The results are shown in Fig. 2.6.6. The inset on Fig. 2.6.6 shows the geometry of the region, which contained two parallel <110> cracks which for convenience have been specified as lying parallel to [110]. Distances were thus measured along the orthogonal [1$\bar{1}$0]. Features to note on Fig. 2.6.6 are that the λ peak shift appears to cease at ~35μm distance from the crack and that the CL intensity maximum occurs over a region up to 5μm from the crack, as already noted in Table 2.6.1.

2.6.4 Discussion

2.6.4.1 Optical and CL images

In general, there is agreement between the optical and CL images, as shown in Figs. 2.6.2-2.6.4 and described in detail in Table 2.6.1. However, in interpreting these images it must be appreciated that the optical micrographs represent images of defects and topological features which were present in the material which was then removed by the etch (the memory effect). In contrast, the CL images arise from a volume of material beneath the surface which has not yet been exposed by the etchant. Fig. 2.6.7 shows this volume schematically. For the 20kV beam employed the penetration depth Rp ~1.5μm in GaAs, so that the effective CL emitting volume extends ~1μm from the surface, neglecting the small intensity emitted beyond this depth. This difference in

sample volume between optical and CL methods explains the differences, for example in images of the unetched surface and the 325 etched surfaces, evident in Table 2.6.1. Clearly no dislocations normal to the surface can be seen, without etching, by the optical examination, but the CL reveals $\sim 10^7 cm^{-2}$ dark spots, which represent the non-radiative dislocation regions.

Indeed, this is subsequently confirmed by the occurence of similar defect densities, after etching, as etch pit densities are $\sim 10^7 cm^{-2}$. It is interesting to note that the CL dark spots are not evident after a brief (10s) etch. This is possibly due to interference from both dark lines and an enhanced surface structure background. The 32s etched optical micrograph still indicates a measurable cross-hatch pattern: the low temperature CL image shows vestigial cross-hatch images too faint to be measured.

By comparing both sets of images some tentative deductions regarding the cross-hatch patterns can be made. Firstly it is clear from both optical and CL images that although cross-hatch is normally defined as a surface effect it seems to be associated with a considerable volume of cross-hatch like defects. Thus optical and CL images both indicate cross-hatch visibility down to $\sim 3\mu m$, perhaps enhanced by the etchant in the case of the optical images, but not in the case of the CL images. Indeed the CL image of the unetched layer (Fig. 2.6.2) indicates dark lines $\sim 10\mu m$ long in [110] and [1$\bar{1}$0] forming a cross-hatch pattern. It is probable that those dark lines appear on the well-defined cross-hatch pattern seen optically after the 10s etch. It is suggested that the cross-hatch pattern results from an array of [110] and [1$\bar{1}$0] dislocations which are distributed throughout $\sim 3\mu m$ depth for the structure of OA^23, and that the surface cross-hatch detected by Nomarski interference contrast microscopy results from glide of the horizontal new surface arrays to form limited extent ($\sim 10\mu m$) slip steps, possibly enhanced by image force attractions to the surface. This cross-hatch network throughout the upper $\sim 3\mu m$ is in additon to the networks evident by plan view and cross-secton TEM examinations, which demonstrate considerably higher, but more confined, dislocation densities at the strained layer superlattice regions.

2.6.4.2 CL peak wavelength shifts in vicinity of cracks

The intrinsic energy gap of GaAs at 300K is E_i=1.442eV and this alters to E_i=1.519eV at 10K (Thurmond 1975) [5]. It also alters under pressure, as:

$$\frac{dE_i}{dP} = +0.0126\text{eV/kbar} \qquad (1)$$

according to Blakemore (1982) [6], although other authors give slightly different values. Pollak and Cardona (1968) report a value of 11.5meV/kbar for the [001] direction and 12.0meV/kbar for the [110] direction, while Yacobi et al (1988) [7] give 10.23meV/kbar for in-plane biaxial tensile stress. The existence of in-plane biaxial tensile stress has recently been demonstrated by Lum et al (1988) [8] for GaAs on Si films grown by MOCVD methods. Measured in-plane strains by double crystal X-ray diffraction were consistently lower than those calculated from thermal expansion mismatch values, and the conclusion was that the formation of cracks provided a mechanism for strain relief. The presence of biaxial tensile stress, as well as altering the band gap energy, removes excitonic-to-valance band degeneracy which results in two CL peaks, reported by Yacobi et al (1987) [4] at 828.7nm (1.496eV) and 823nm (1.506eV). Careful examination of the 10μm curve in Fig. 2.6.5 indicates that two overlapping peaks are present, at ~830nm and ~820nm, but we shall ignore this in the following simple treatment.

According to Blakemore (1982) [6] the bulk modulus (k) for GaAs=7.55×10^{11} dyne cm^{-2} and shear modulus (G)=3.26×10^{11} dyne cm^{-2}. From these values Youngs modulus (E) can be determined from:

$$E = \frac{9kG}{G+3k} \qquad (2)$$

giving E=8.54×10^{11} dyne cm^{-2}

The low temperature CL peak λ is constant at distance ~>30μm from a <110> crack at 1.488eV (833.0nm). At the crack the CL peak λ is 1.506eV (823nm). thus the measured shift is -18.0meV. Using the Yacobi et al (1988) value of 10.23meV/kbar, this corresponds with a pressure of 1.760 kbar=1.760×10^{9} dyne

cm^{-2}. The negative sign in the shift indicates that at distances >30μm from cracks the material is under tensile strain.

The magnitude of the strain is then simply obtained from Hooke's Law

$$E = \text{stress}/\text{strain};\ \text{with stress}=1.760\times10^{9}\ \text{dyne cm}^{-2},\ E=8.54\times10^{11}\ \text{dyne cm}^{-2}$$

$$\therefore\ \text{strain} = \frac{1.760\times10^{9}}{8.54\times10^{11}} \times 100\% = 0.21\% \qquad (3)$$

The stress value of 1.760 kbar is in good agreement with the value of "about 1.8kbar in the central reigon of the cell" quoted by Yacobi et al (1987).

It is interesting to compare our strain magnitude with those determined for the strain in Ford and Plessey samples using the photoreflectance (PR) method reported by Bottka et al (1988) [9]. The Ford samples gave an energy gap shift $\delta\varepsilon_i$=14meV, which the authors equate with a strain of 0.23%, whereas the Plessey samples gave a much smaller shift of $\delta\varepsilon_i$=7meV corresponding to a strain of 0.11%. [Note there is a discrepancy between the relation of $\delta\varepsilon_i$ to strain compared with our values calculated from equations (1)-(3)]. The values obtained were used to predict the epitaxial growth temperatures from ternary values of the elastic constants and thermal expansion coefficients. Because prediction was poor for the Plessey samples, although good for the Ford samples, it was concluded that some portion of the cooling strain in the Plessey layers was being relieved, and the mechanism was suggested to be by reduction at the strained layer superlattice/GaAs interfaces. However, the results reported here suggest that an alternative explanation may be the presence of <100> cracks, which as we have seen will also relieve some of the strain. It is interesting to note that the PR method is essentially a large area technique, in which ~70% of the epitaxial layer area is measured, thus encompassing many zero strain cracks in addition to areas remote from cracks. Thus the strain measured by PR is expected to lie between 0% and 0.21%.

3. DEVICES

3.1 FET Fabrication

The four latest wafers of MOCVD-grown material were processed as test FETs, using the same mask set as on the previous experiments. Two wafers were of GaAs on GaAs (OA652, OA657) and two of GaAs on Si (OA653, OA664). The surfaces of the GaAs on GaAs wafers were good, although some "parachutes" were visible on OA652. The GaAs on Si surface morphology was less smooth, with fine cracks evident along the <110> directions, arising from thermal expansion mismatch. In addition, these wafers exhibited significant bowing of up to 40μm centre to edge in 300μm thickness. This factor, combined with the fact that these were part-wafers, posed considerable lithographic problems at the gate stage, resulting in reduced device yields.

Mesa isolation, previously a problem with GaAs on Si, was acceptable for device fabrication on most of the GaAs on GaAs wafers but still not adequate on the GaAs on Si. For the standard Plessey test of probing between two mesas 20μm apart, GaAs on GaAs isolation was 10μA at 40V applied, whereas the GaAs on Si measured only 2-5V for the same current. One of the GaAs on GaAs wafers (OA652) was also more light-sensitive than normal for this test, with partial breakdown occurring at 10V. In all cases the wet chemical mesa etch was continued to a depth calculated to be well into the buffer layer.

Ohmic contacts were prepared on all the wafers, with good contact resistances, 0.2Ω mms, being measured. Saturation current for the 150μm wide test FET was measured and revealed the familiar patterns of non-uniformity typical of epitaxial growth, Figs. 3.1.1. The non-uniformity of the GaAs on Si devices was more random than that of the GaAs on GaAs, but this may be a function of the poor mesa isolation, since devices were also prone to breakdown during test. The spread of I_{sat} values recorded was also more than twice that of the GaAs on GaAs devices.

The two GaAs on Si wafers produced very poor FETs due to the inadequate device isolation. The breakdown of the gate Schottky was very "soft" and this leakage resulted in devices which failed to pinch off, Fig. 3.1.2. It

was possible to measure transconductance g_m near I_{dss} on one of the wafers (OA664) and 110mS/mm was typical. This compares with 125mS/mm (typical) on wafer OA407, reported earlier in this programme. The GaAs on GaAs FETs d.c. characteristics are shown in Fig. 3.1.3. The g_m of these devices was 155mS/mm typical, with peak extrinsic values of 175-190mS/mm, Fig.3.1.4. The GaAs on GaAs wafers were diced for microwave test after provision of bond pad overlay metallisation. Half of each wafer was passivated with silicon nitride prior to thinning.

4. CONCLUSIONS

(1) Encouraging results have been obtained for low temperature (950°C) substrate cleaning using a microwave generated plasma with arsine hydrogen mixtures at 5 Torr.

(2) Assessment of FET devices in GaAs on silicon has highlighted problems associated with obtaining reproducible growth of high resistance buffer layers.

(3) Cathodoluminescence studies have shown that GaAs on silicon layers are under tensile strain, and that the cracks alongs <110> relieve the strain completely at the crack with diminishing effectiveness over distances ~30μm from the cracks.

(4) A further batch of silicon substrates has been processed ready for growth on profiled substrates.

(5) Comparison of simultaneous growth of GaAs on exact (001) and (001) tilted 3° towards the furthest (110) silicon substrates has revealed significant differences in layer morphology and background doping.

5. FUTURE PROGRAMME

(1) Continue growth and assessment of GaAs/Si FETs.

(2) Continue development of low temperature (~900^{0}C) silicon substrate cleaning techniques.

(3) Carry out further growth on profiled silicon substrates using recently prepared material.

(4) Investigate and assess the use of in-situ cyclic thermal annealing as a means of improving material quality.

(5) Carry out further investigations of the effect of silicon substrate orientation on layer nucleation, surface morphology, and electrical properties.

(6) TEM studies of initial layer nucleation of GaAs on silicon.

(7) Design of low complexity structures containing more than one device structure depending on progress in the development of low temperature cleaning procedures in (2).

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TABLE 2.6.1

OPTICAL AND CL IMAGE COMPARISON AT DIFFERENT ETCH DEPTHS

ETCH TIME (S)	ESTIMATED ETCH DEPTH (μm)	OPTICAL MICROGRAPHIC IMAGES	10K CL IMAGES
0	0	Narrow cracks ~0.2μm wide // [110] Faintly visible cross-hatch Pronounced surface structure	Narrow cracks (dark contrast ≡ 1mW emission) ~0.25μm wide flanked by 5μm strips showing enhanced emission. Dark spot density $\sim 10^{7}cm^{-2}$ Dark line density along [1$\bar{1}$0], ⊥ cracks $\sim 3x10^{3}cm^{-1}$; along [110]//cracks $\sim 10^{3}cm^{-1}$ Corresponding surface structure, contrast enhanced in 5μm wide strips at cracks.
10	1	Most cracks opened to ~3.5μm widths (but not all - see Fig. 2.4.2). Etch pit densities $5x10^{6}cm^{-2}$ Well defined cross-hatch $\sim 5x10^{3}cm^{-1}$ density along [110] and [1$\bar{1}$0]. Pronounced surface structure.	Crack width ~1μm, still flanked by 5μm wide enhanced emission strips. Dark spots no longer evident. Dark line density along [1$\bar{1}$0]/⊥ cracks $\sim 5x10^{3}cm^{-1}$, along [110]//cracks - faint. Corresponding surface structure, enhanced new cracks.
20	2	Cracks further enlarged to ~4.0μm. Etch pit density $\sim 3x10^{7}cm^{-2}$. Well-defined cross-hatch $\sim 10^{4}cm^{-1}$. along [110] and [1$\bar{1}$0] No surface structure visible.	Crack width ~1.8μm, with 5μm wide enhanced emission strips. No dark spots evident. Well-defined cross-hatch $\sim 10^{4}cm^{-1}$ along [110] and [1$\bar{1}$0]. No surface structure visible.
32	3.2	Cracks enlarged to ~5.0μm. Etch pit density $\sim 3.6x10^{7}cm^{-2}$. Cross-hatch $\sim 1.3x10^{4}$cm-1 along [110] and [1$\bar{1}$0]. No surface structure.	Crack width ~3.0μm, with 5μm wide enhanced emission strips. No dark spots evident. Cross-hatch just detectable but not measureable. No surface structure.
44	4.4	Cracks enlarged to ~7.0μm. Etch pit density $\sim 5x10^{7}cm^{-2}$. (difficult to estimate because over-etched) Cross-hatch also appears over-etched but otherwise similar to 32s region. No surface structure.	Crack width ~5.0μm, with 5μm wide enhanced emission strips. Complex background structure: no detectable cross-hatch but a mottled mixture of dark and light regions. No surface structure.

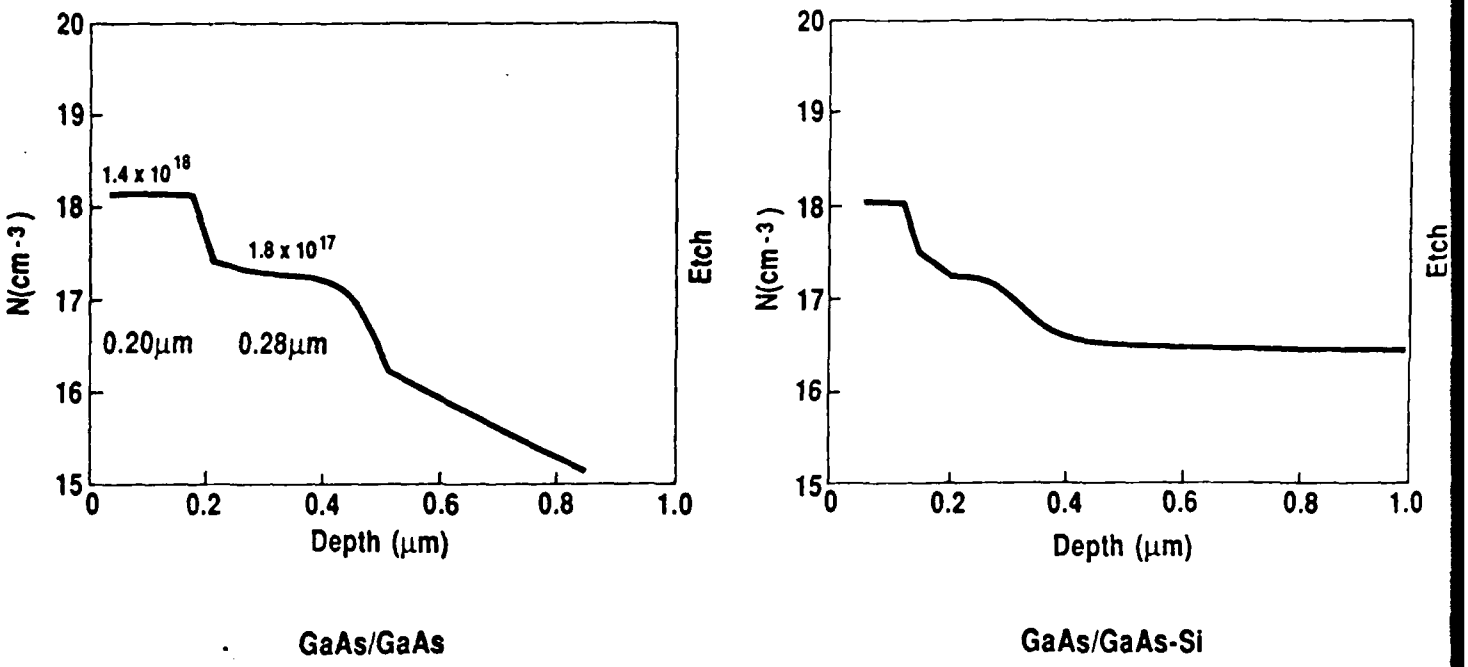


Figure 2.1.1 (a) POP PROFILES OF FET STRUCTURE ON GaAs, AND ON GaAs ON Si (2 step growth)

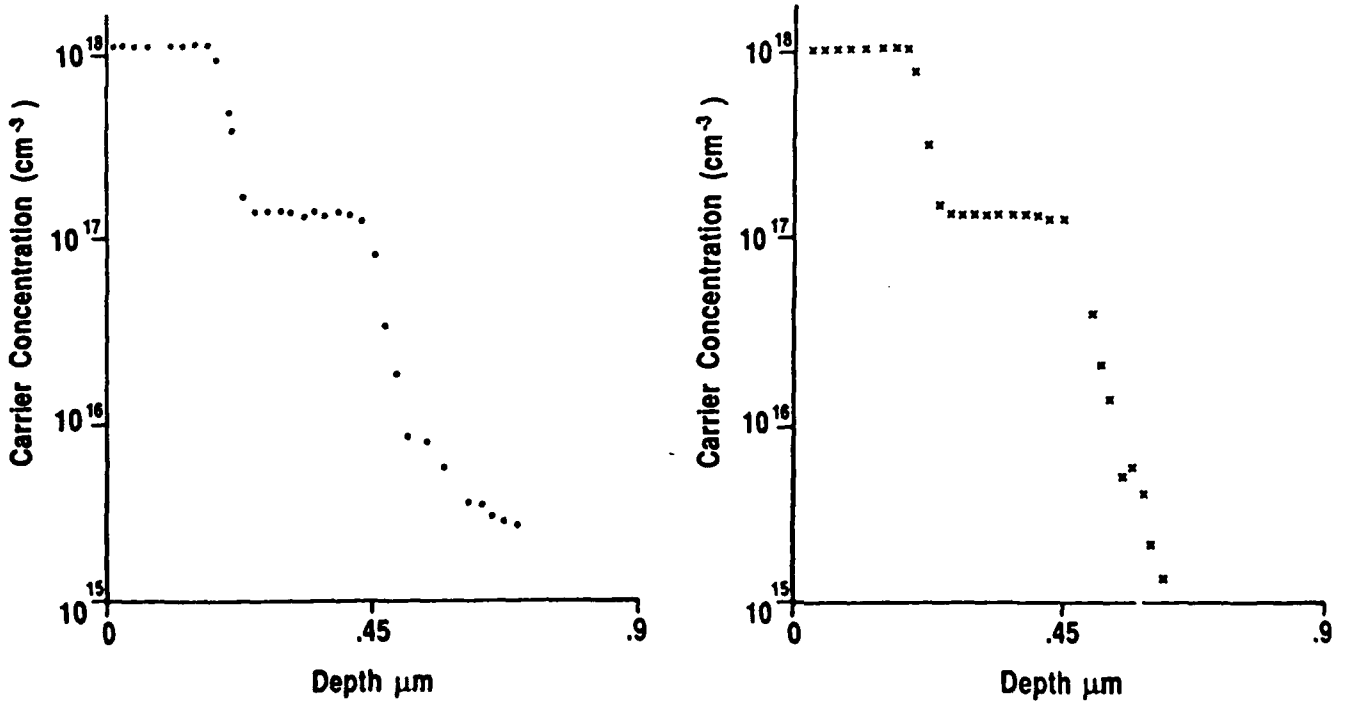
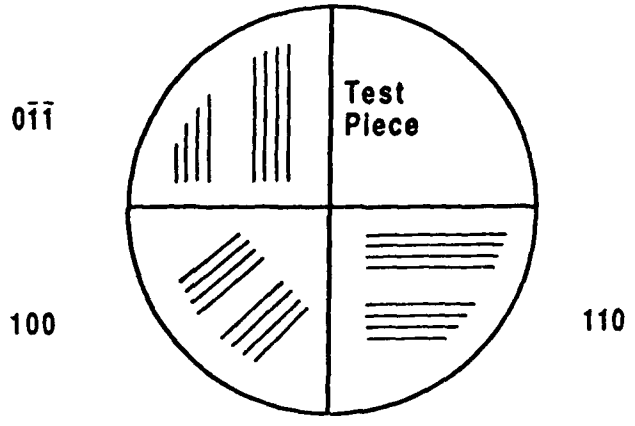


Figure 2.1.1 (b) (i) GaAs ON SILICON FET

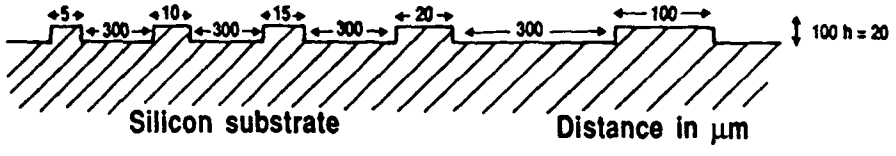
Figure 2.1.1 (b) (ii) GaAs/GaAs FET

3" diameter wafer cleaved into 4 pieces. Stripe orientation as shown



Wet and dry etched specimen prepared. Si_3N_4 Mask

Fig. 2.3.1. SUBSTRATE PREPARED FOR GROWTH ON PROFILED SUBSTRATES



The mask used to prepare these substrates has a series of stripes, 5, 10, 15, 20 and 100μm wide with a spacing of 300μm between them.

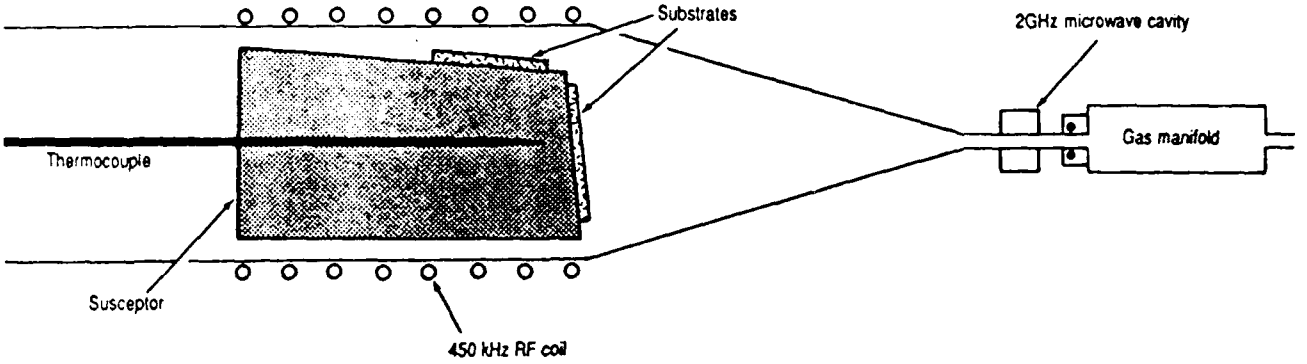
Ribs are prepared by either wet chemical etching or dry etching techniques.

Ribs used for these experiments were 2.0μm high.

Wet chemical etch used for silicon → 2% HF in HNO_3.

Dry etching of silicon substrates → reactive ion etch in CF_4.

Fig. 2.3.2. RIBBED STRUCTURE USED FOR GROWTH ON PROFILED SUBSTRATES



Advantage : Good plasma propagation and transport of reactive species
Better interaction of reactive species and vertical substrate
Better RF coupling to susceptor enables higher temperature to be used

Fig. 2.4.1. HORIZONTAL AND VERTICAL MICROWAVE - RF PLASMA CLEANING ARRANGEMENT

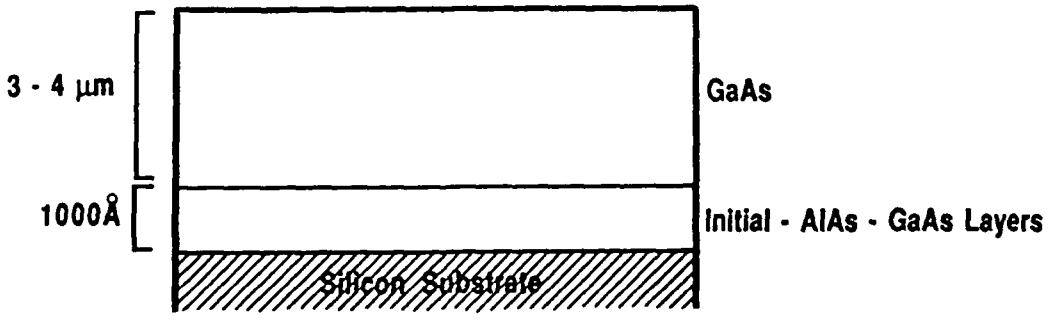


Fig. 2.4.2. TYPICAL STRUCTURE Grown after microwave R.F. plasma cleaning

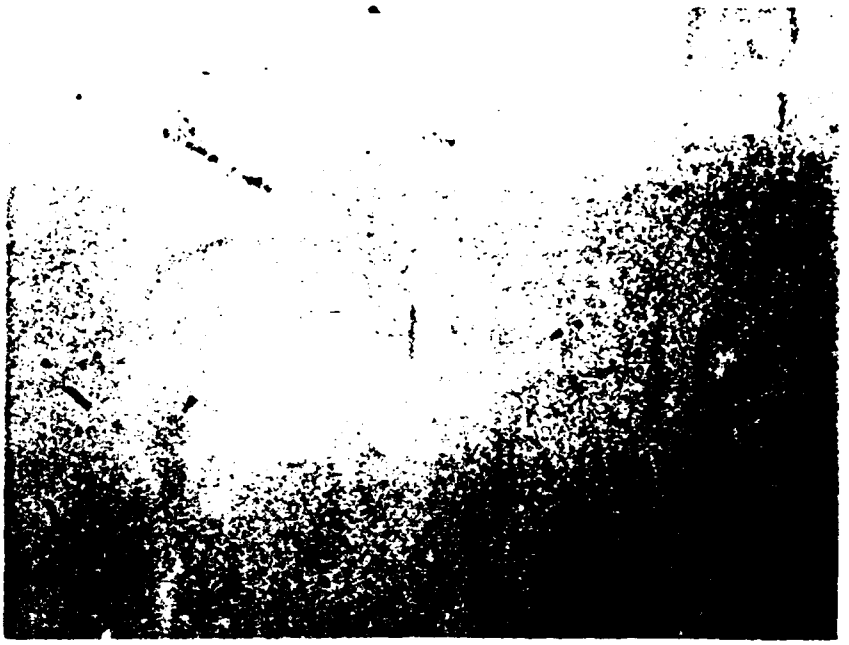


Fig. 2.4.3. NOMARSKI INTERFERENCE CONTRAST OPTICAL MICROGRAPH OF RF PLASMA CLEANED GaAs on Si

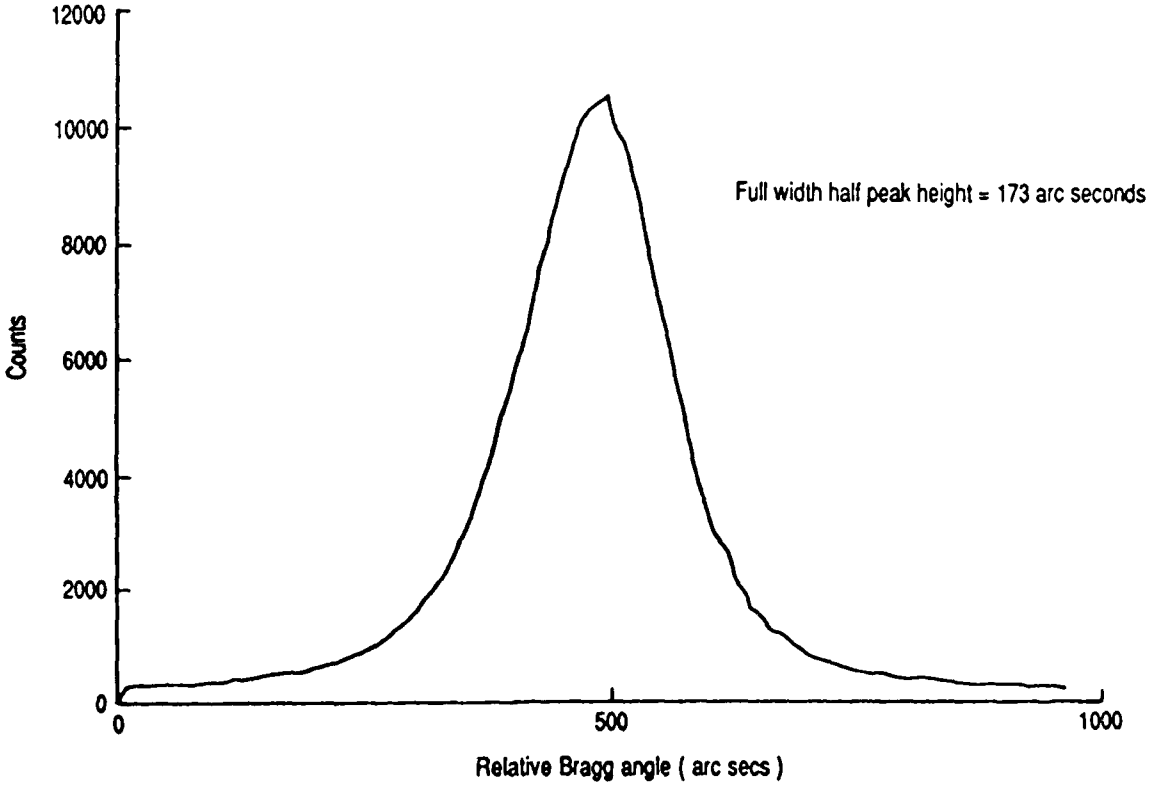


Fig. 2.4.4. MICROWAVE PLASMA CLEANED SAMPLE OF GaAs ON Si
Experimental Rocking Curve

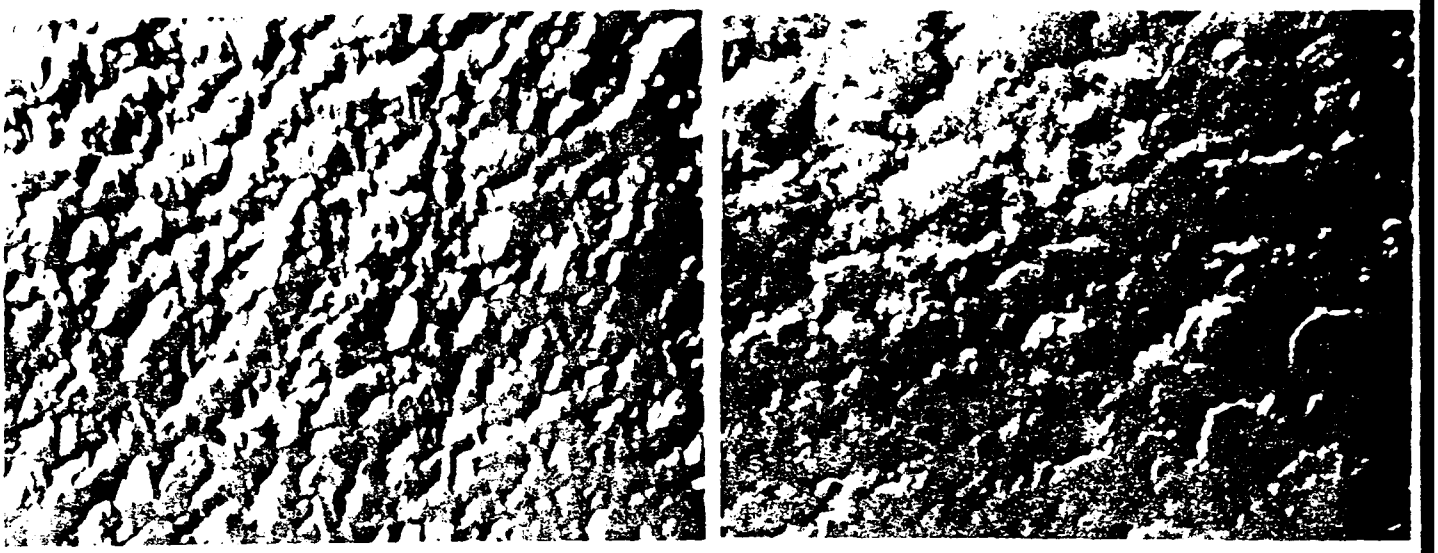
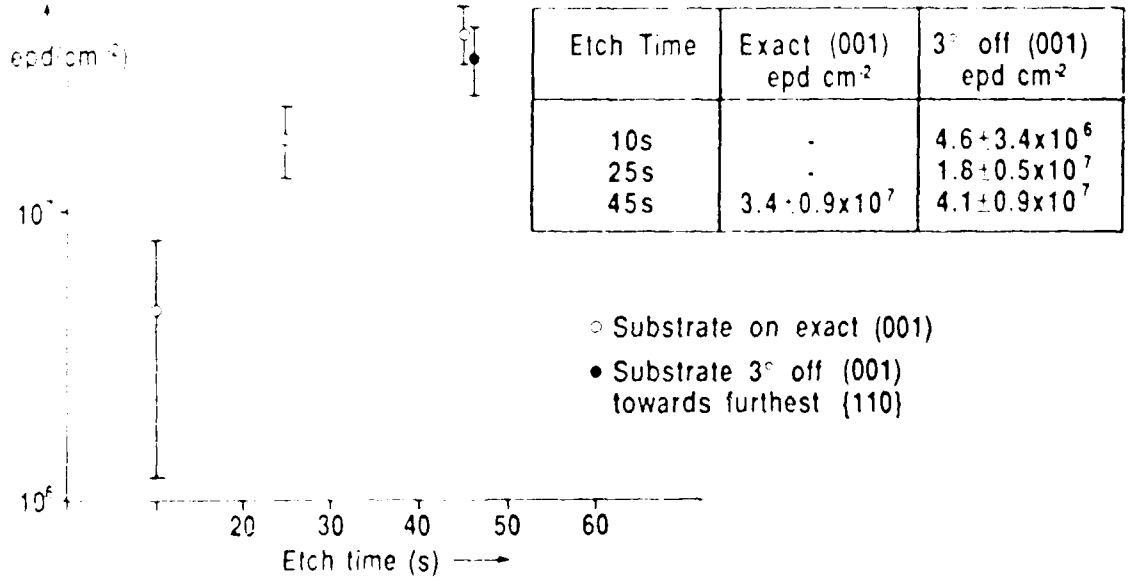


Fig 25 OPTICAL MICROSCOPY SHOWING DIFFERENCE IN SURFACE MORPHOLOGY



Etch Time	Exact (001) epd cm⁻²	3° off (001) epd cm⁻²
10s	-	$4.6 \pm 3.4 \times 10^6$
25s	-	$1.8 \pm 0.5 \times 10^7$
45s	$3.4 \pm 0.9 \times 10^7$	$4.1 \pm 0.9 \times 10^7$

Fig 252 IDENTICAL GROWTH OF TWO HALF-SUBSTRATES WITH DIFFERING ORIENTATIONS

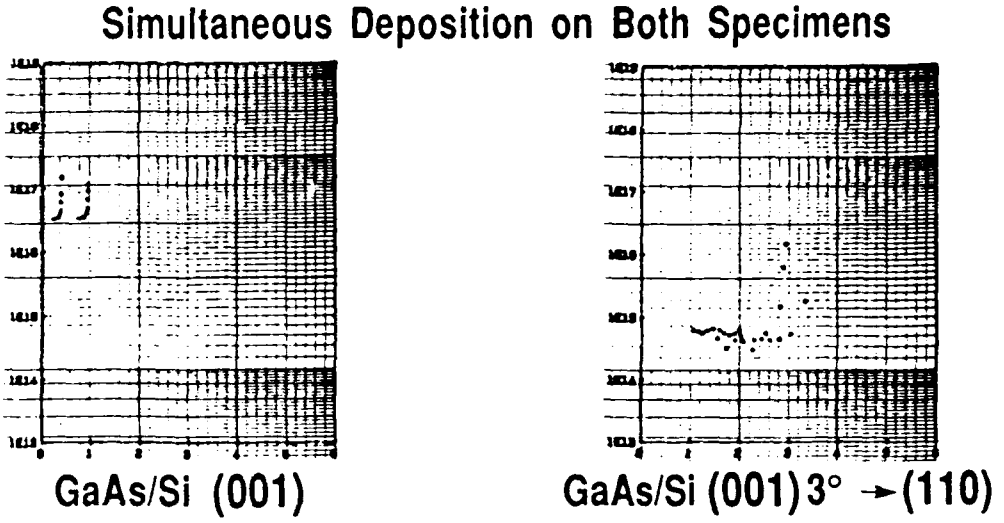


Fig. 2.5.3. COMPARISON OF CV PROFILES FOR GaAs/Si (001) AND GaAs/Si (001) 3° → (110)

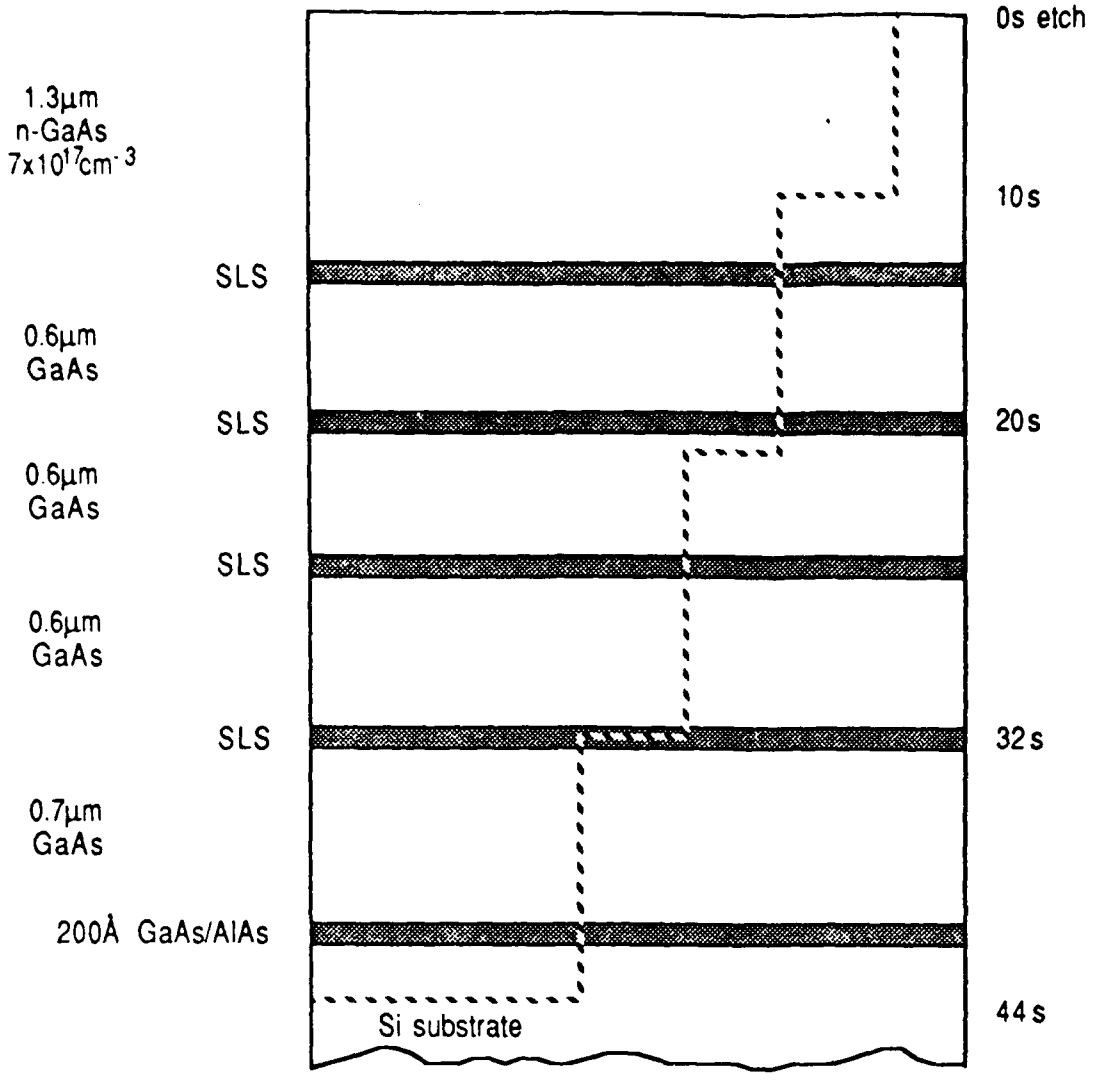


Fig. 2.6.1. STRUCTURE OF OA 423 EPILAYERS. ETCH DEPTHS ASSUMMING CONSTANT REMOVAL RATE OF 0.1μms^{-1} SHOWN AS DOTTED LINE

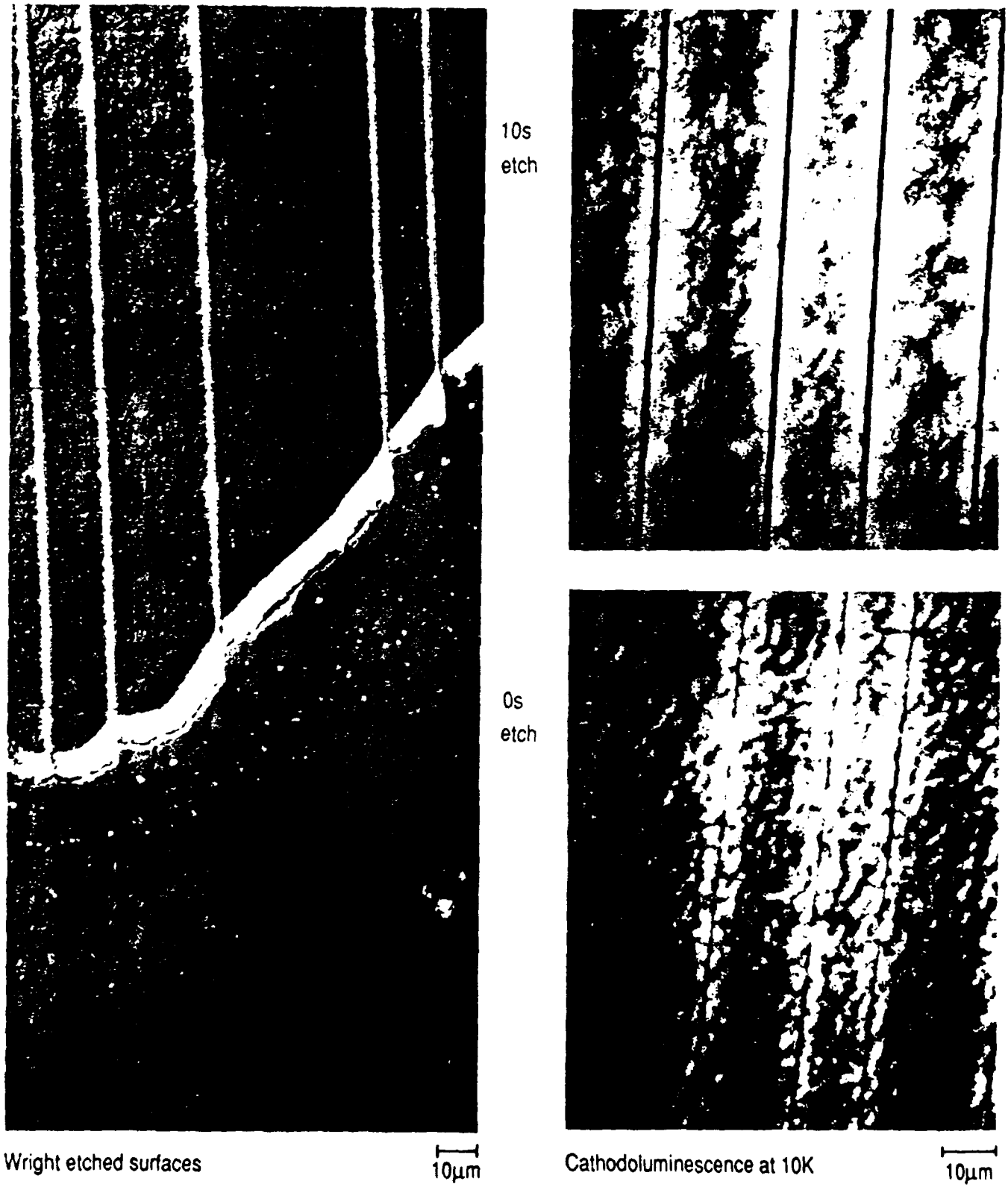


Fig. 2.6.2. Etched surface micrographs and CL emission for 0s and 10s etch areas.

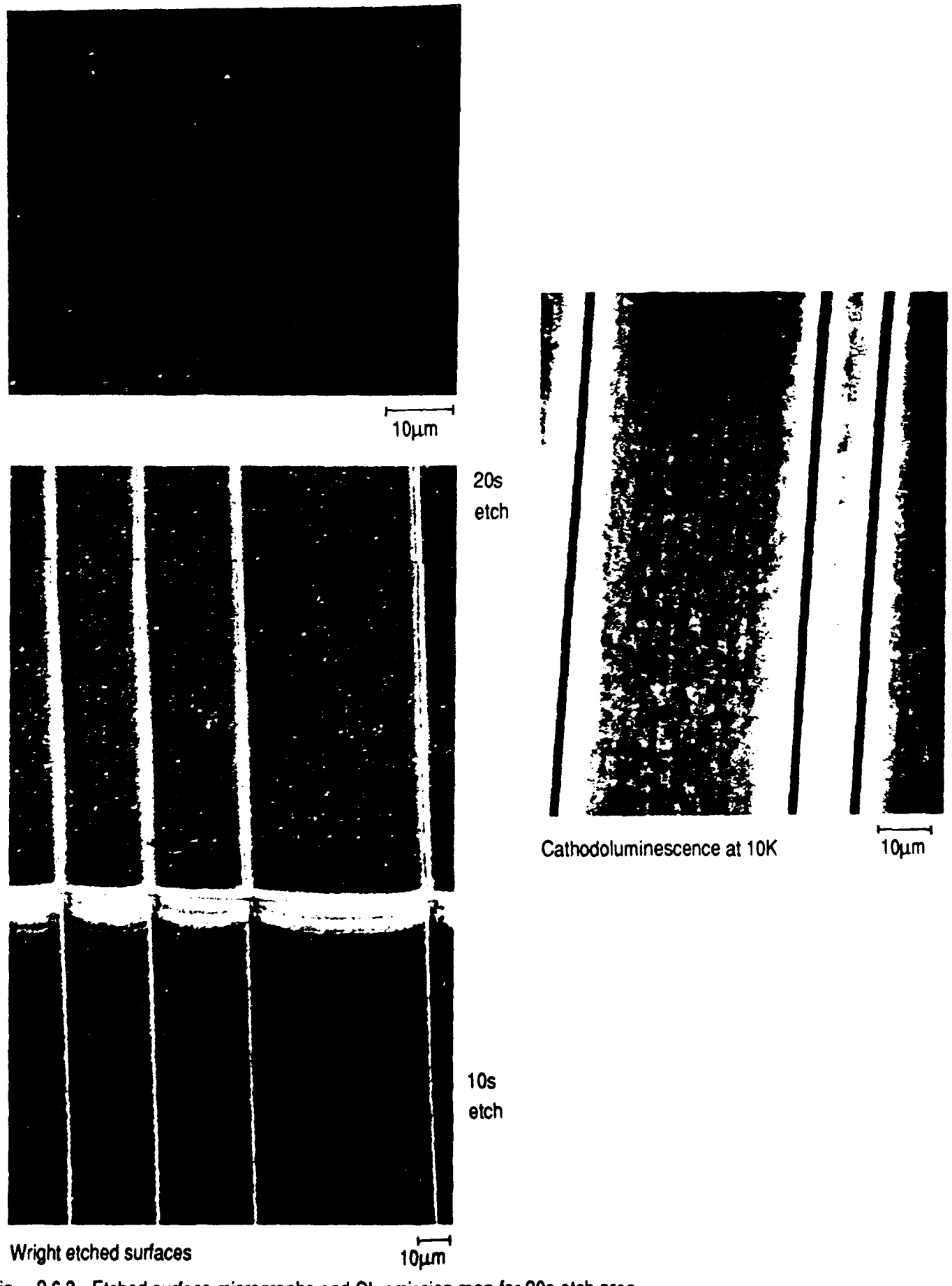


Fig. 2.6.3. Etched surface micrographs and CL emission map for 20s etch area

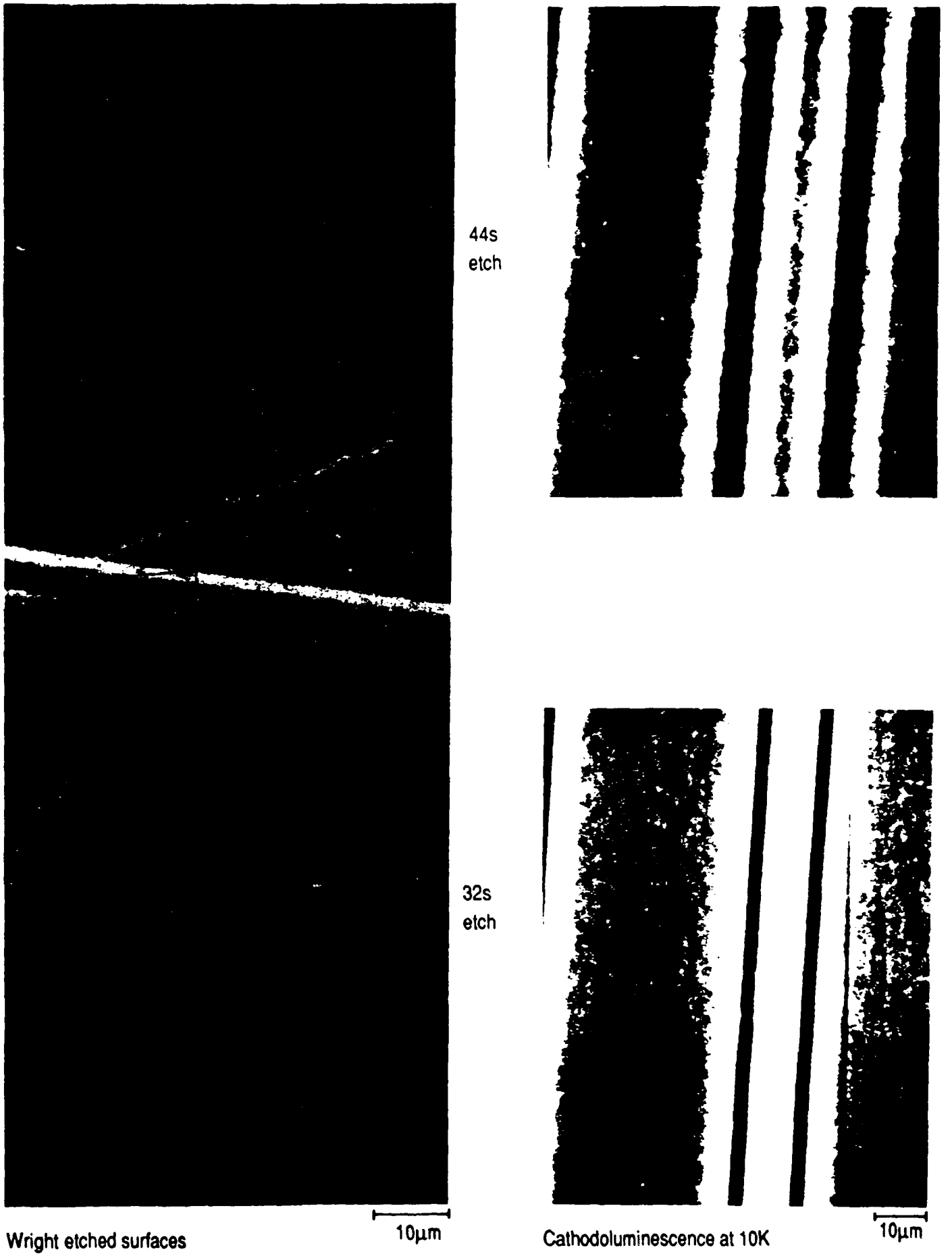


Fig. 2.6.4. Etched surface micrographs and CL emission maps for 32s and 44s etch areas.

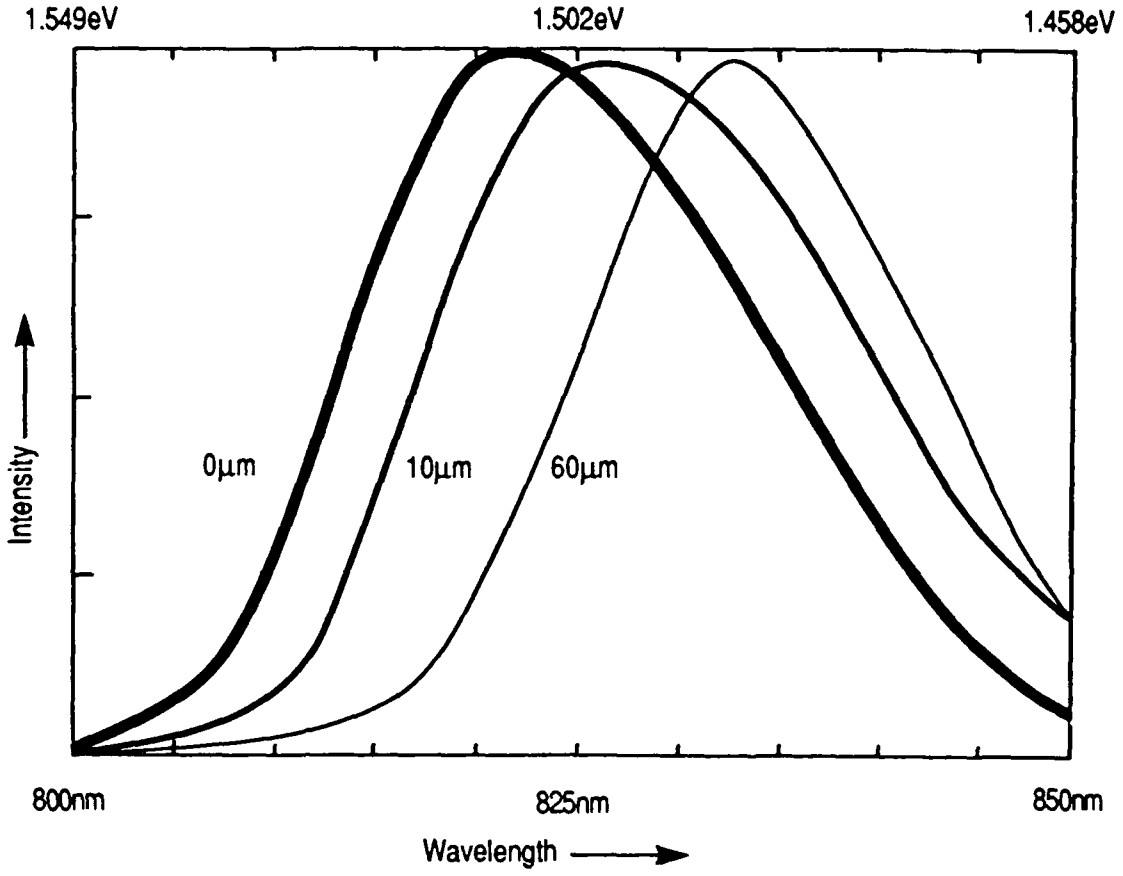


Fig. 2.6.5. SHIFT OF PEAK CL WAVELENGTH WITH DISTANCE FROM CRACK (in μm)
Note that the peak heights are not scaled with peak intensities

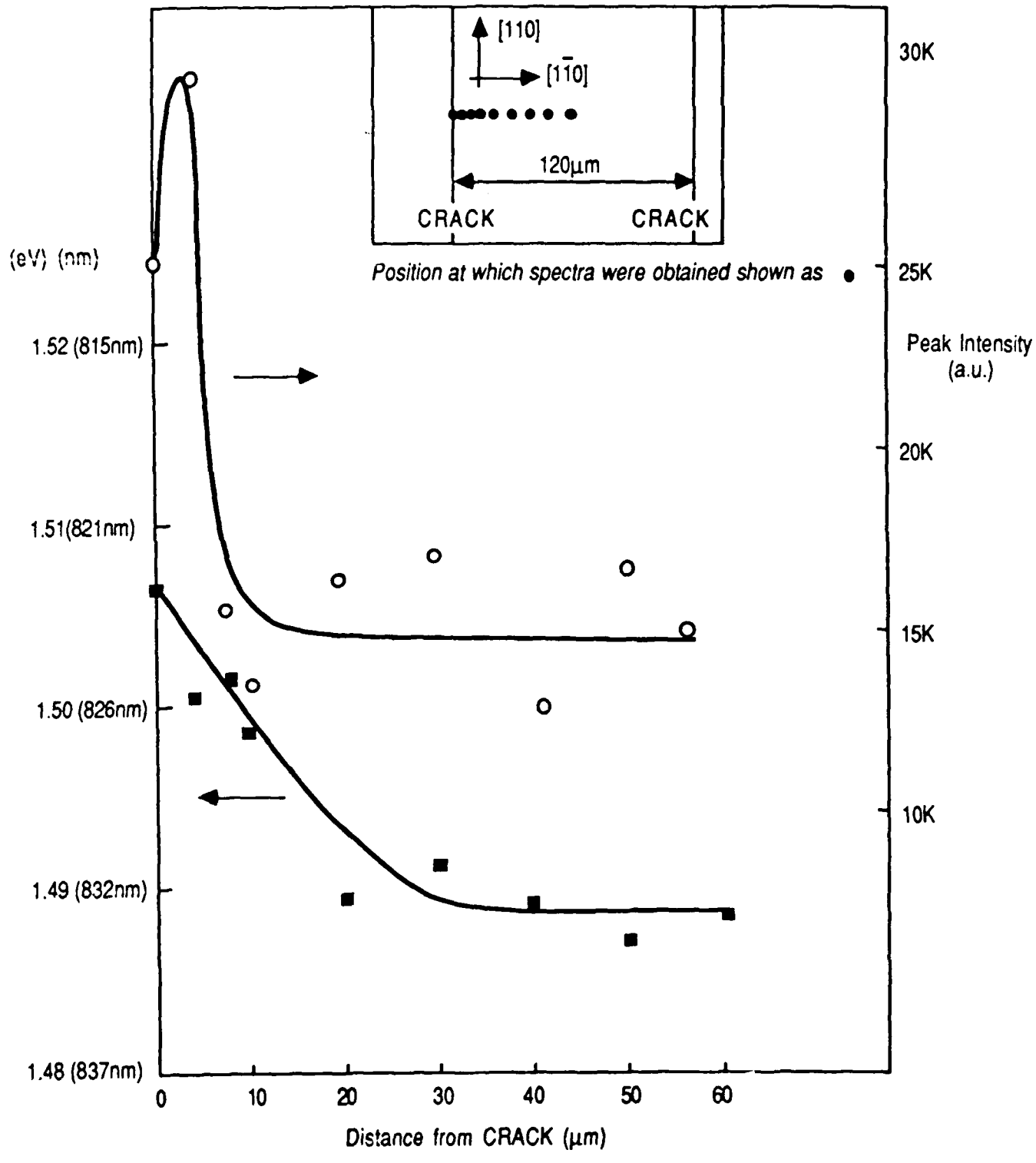


Fig. 2.6.6.

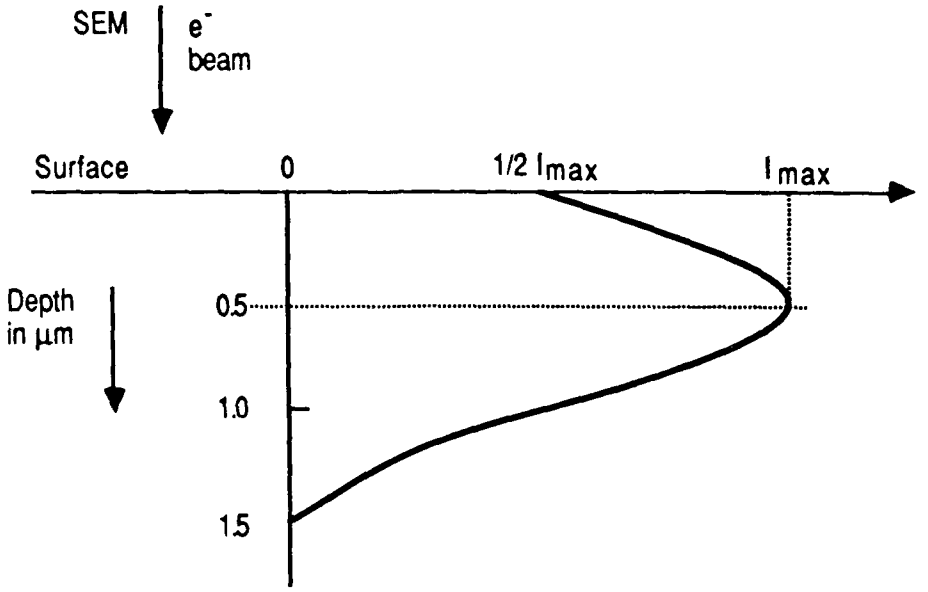
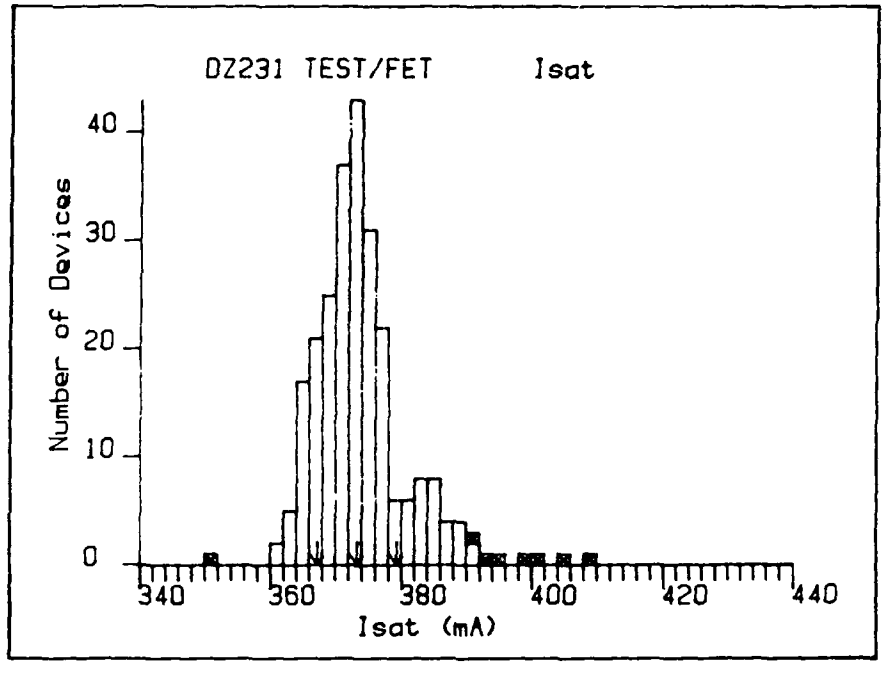


Fig. 2.6.7. VARIATION OF CL INTENSITY I WITH PENETRATION DEPTH OF ELECTRON BEAM

```
                1         2         3
    345678901234567890123456789012345678 9

 0                  2 2 2 3 3 2 2 3 3 3
 2              4 3 3 4 3 3 3 3 3 3 2 3 3 4
 4            5 5 5 4 3 3 3 4 4 3 3 3 3 4 4 4
 6          6 5 5 5 5 4 4 4 4 3 4 3 3 4 4 4 4 /
 8          6 6 5 5 5 4 4 4 4 4 4 4 4 4 4 4 4 /
10  /       6 6 6 5 5 5 4 5 4 4 4 4 4 4 4 4 5 4
12  7       7 7 6 6 5 5 4 5 4 4 4 4 4 4 4 4 4 4
14  7       8 7 6 5 5 5 4 4 4 5 4 4 4 4 4 4 4 4
16  8       7 7 7 6 5 5 5 5 5 4 4 5 4 4 4 4 3 4
18  /       7 7 6 5 4 5 5 4 5 5 4 3 4 4 4 3 3 4
20            6 6 6 6 5 4 5 4 4 4 4 3 3 4 4 3 3 3
22            / 6 5 5 4 4 4 4 4 4 3 4 3 3 2 3 3 7
24              6 5 4 4 4 4 4 3 4 3 3 3 3 2 2 4
26                6 4 2 4 3 2 3 2 3 3 3 2 2 6
28                    4 / 3 3 3 3 2 2 2 3
30                        / / / / / /
```

KEY: Isat (mA)

```
< : <= 350
0 : >350, <= 355
1 : >355, <= 360
2 : >360, <= 365
3 : >365, <= 370
4 : >370, <= 375
5 : >375, <= 380
6 : >380, <= 385
7 : >385, <= 390
8 : >390, <= 395
9 : >395, <= 400
> : >400

/ : Fail
```



Mean = 373.174 mA
Sigma = 6.02 mA

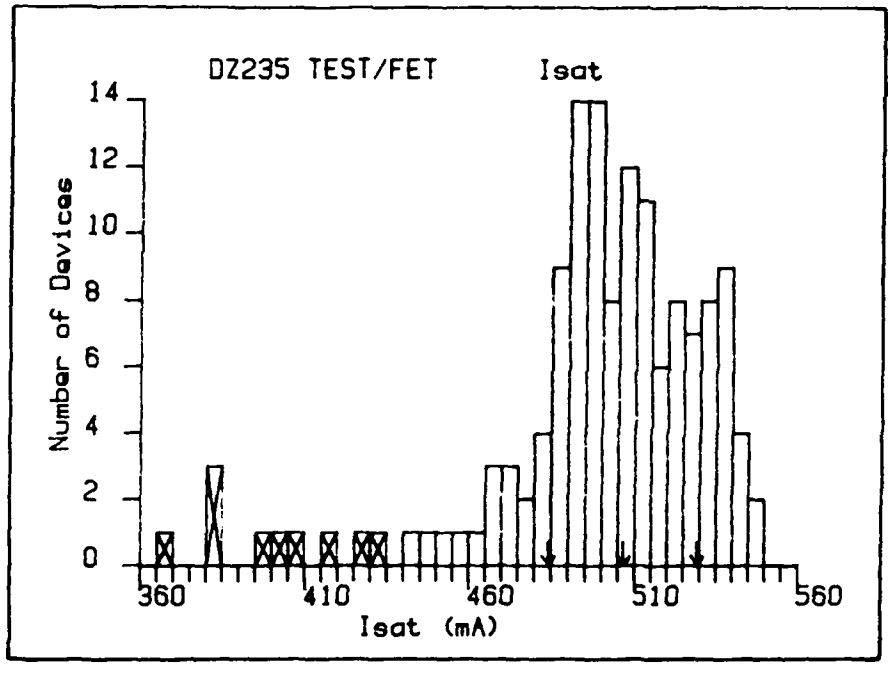
Total no. = 253
Passes = 241
Yield = 95.3 %

Figure 3.1.1 (a) SATURATION CURRENT DISTRIBUTION FOR OA657
(GaAs on GaAs, 1x150µm FET)

```
      1          2
     7890123456789012345678 9

 2                  3 8 8 9 9 9 8
 4                8 8 9 8 9 8 / 8
 6          7 6 / 7 8 7 8 / 5 5
 8        1 6 6 / 7 7 / 6 < 3 8
10        7 6 1 6 6 8 / 8 7 7 /
12    6 6 5 6 7 7 8 / 8 7 8 /
14    / 4 5 5 6 7 6 1 8 7 6 /
16    / 4 3 5 5 6 5 3 7 6 5 0
18    > 3 4 5 5 5 6 0 4 4 4 <
20    / / 4 4 4 5 4 / 2 1 3 2
22    / / / 4 3 5 5 / 4 5 2 4
24      / 3 5 4 4 4 / 4 3 4 /
26      / 7 3 5 4 5 4 4 / 3 /
28        / 9 4 4 4 2 6 4 5 /
30              / 3 3 / 4 4 4 2
32                / / / / / / /
```

KEY: Isat (mA)

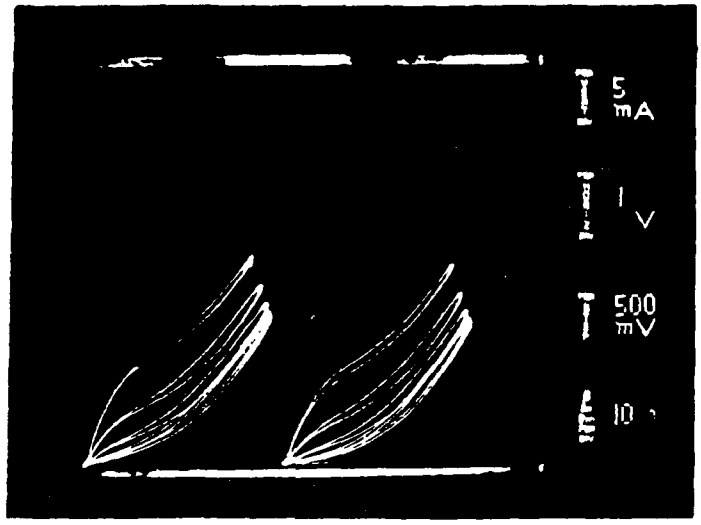
```
< : <= 450
0 : >450, <= 460
1 : >460, <= 470
2 : >470, <= 480
3 : >480, <= 490
4 : >490, <= 500
5 : >500, <= 510
6 : >510, <= 520
7 : >520, <= 530
8 : >530, <= 540
9 : >540, <= 550
> : >550

/ : Fail
```



Mean = 506.599 mA
Sigma = 22.49 mA

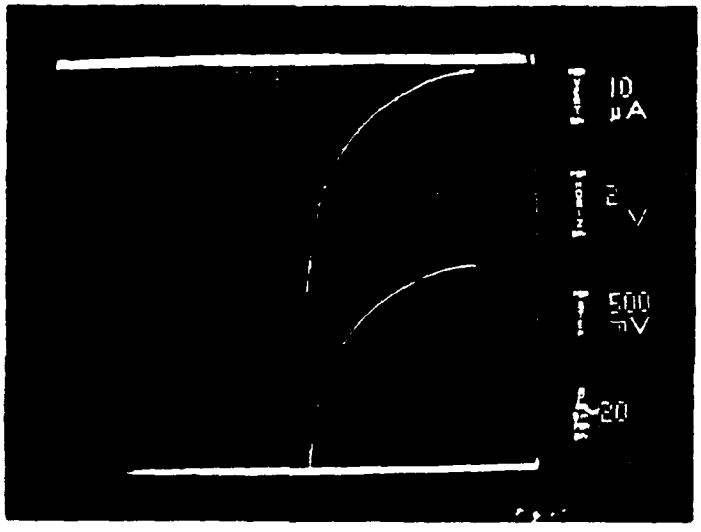
Total no. = 166
Passes = 130
Yield = 78.3 %

Figure 3.1.1 (b) SATURATION CURRENT DISTRIBUTION FOR OA664
(GaAs on Si, 1x150µm)



OUTPUT CHARACTERISTICS

LIGHT ON LIGHT OFF



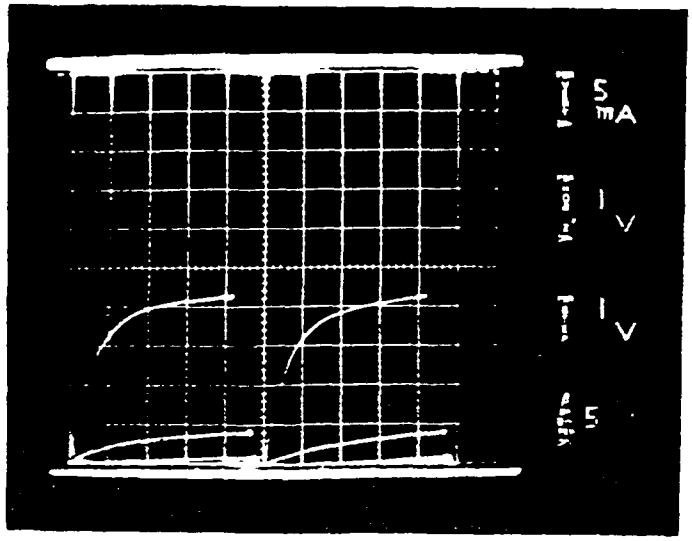
LIGHT ON

LIGHT OFF

DIODE REVERSE CHARACTERISTIC

V_D = 8 V

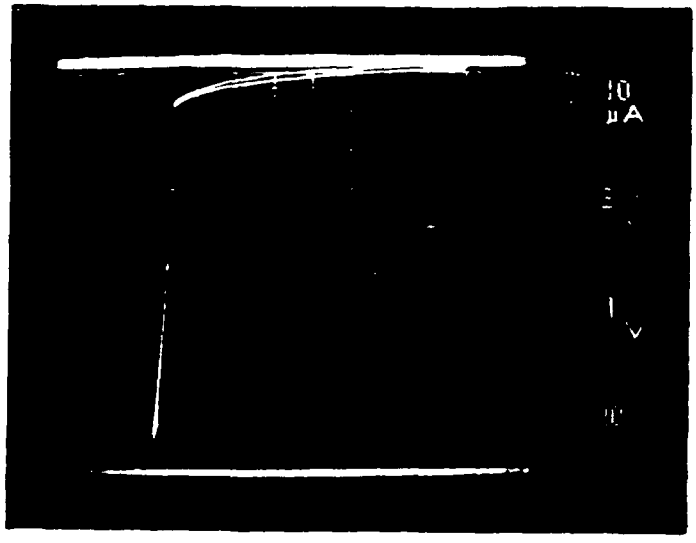
Figure 3.1.2 OA653 (DZ234) UNPASSIVATED 1x150µm FET - GaAs on Si



OUTPUT CHARACTERISTICS

Gm = 115 mS/mm

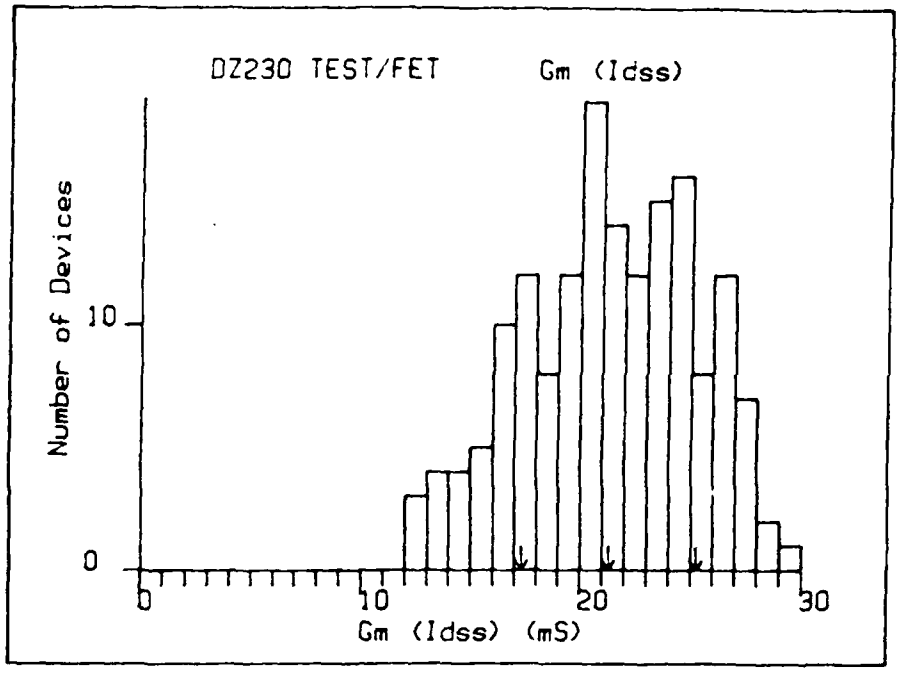
LIGHT ON LIGHT OFF



DIODE REVERSE CHARACTERISTIC

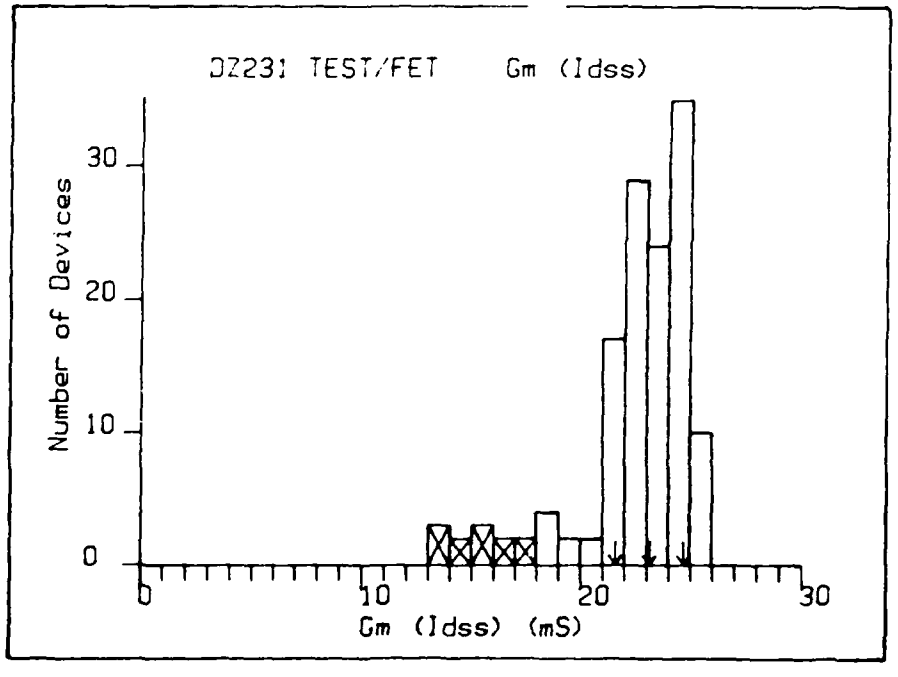
Vb = 15 V

Figure 3.1.3 OA657 (DZ231) UNPASSIVATED 1x150µm FET - GaAs on GaAs



Mean = 21.26 mS
Sigma = 3.97 mS

Total no. = 254
Passes = 164
Yield = 64.6 %



Mean = 23.11 mS
Sigma = 1.55 mS

Total no. = 254
Passes = 123
Yield = 48.4 %

Figure 3.1.4 COMPARISON OF TRANSCONDUCTANCES FOR 1x150µm GaAs on GaAs FETs (OA652 = DZ230, OA657 = DZ231)